

## 2.0 BUS DESCRIPTION AND PROTOCOL

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## 2.1 Physical Layer

Figure 2-1 ~~Figure 2-4~~ shows a typical physical layer with the following characteristics:

1. One twisted pair shielded cable
2. EIA-485 Electrical characteristics
3. Range: - 7 Vdc to + 12 Vdc with respect to signal ground (refer to item 11 below)
4. Low Speed: 9.6 kbps  $\pm 1.5\%$
5. Bit rate = Baud rate
6. Non Return to Zero (NRZ) signaling
7. Differential Signaling: A MARK or 1 is indicated by the + line being a minimum of 200 millivolts higher (HI) than the – line. A SPACE or 0 is indicated by the + line being a minimum of 200 millivolts lower (LO) than the – line. The idle state of the line (no connection is transmitting) is a MARK or 1.
8. Maximum cable length: 100 ft.
9. Cable characteristic impedance:  $100 \Omega \pm 10 \Omega$
10. Cable shield tied to chassis ground at both ends
11. Signal Ground options:
  - a. Provided by Master via a single, independent wire (see Notes 1 and 2) as Illustrated in ARINC Specification 809
  - b. Provided by the Chassis Ground/Cable Shield (see Note 1 and ARINC Specification 628 Part 2)
12. Terminated at bus ends only. Alternate methods of termination are acceptable.

Notes:

1. If the Master ties Chassis Ground, Cable Shield, and EIA 485 Signal Ground together, a slave can obtain a common ground reference from Chassis Ground, Cable Shield, or an independent signal ground / common wire from the Master.
2. If the Master isolates EIA 485 Transceiver from chassis ground, the common ground reference for the ARINC 485 interface must be provided by a single, independent wire and all slaves must provide a transceiver whose ground reference is connected to this wire but is isolated from Chassis Ground.

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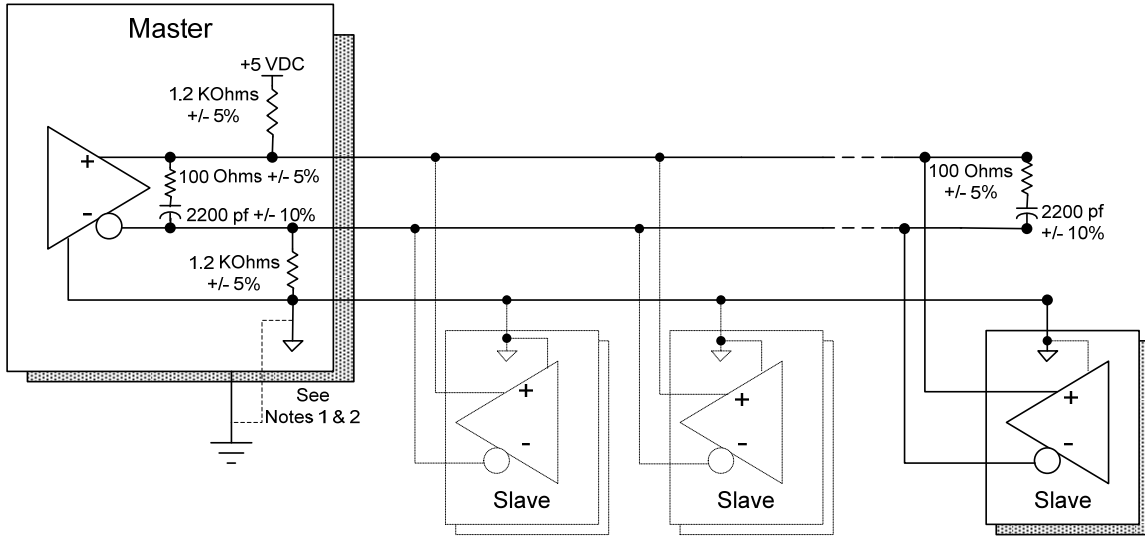


Figure 2-1 - Physical Interface – Typical

**COMMENTARY**

The Physical layer of an ARINC 485 link must have a common ground reference. Damage can occur to interface components if a common reference is absent. Units installed in a seat system must assure that all units on the physical link have a compatible approach toward a common ground reference. Special attention needs to be paid to Slave devices per signal ground option b) in conjunction with a master using signal ground option a) where this signal ground is not equal to chassis ground.

2.2 Data Link Layer

The bus should be asynchronous and half duplex.

2.2.1 Byte Format

The bit definition should be as shown in Figure 2-2 ~~Figure 2-2~~.

1. Byte = 1 Start bit, 8 Data bits, 1 Odd Parity bit, 1 Stop bit
2. Start bit = binary 0 = + line HI, - line LO = Space state
3. Stop bit = binary 1 = + line LO, - line HI = Mark state
4. The LSB of the most significant byte should be transmitted first
5. Inter byte gap (Idle)  $\leq 1$  byte period
6. Idle = + line LO, - line HI